REMARKS

This Amendment is in response to the Office Action mailed September 10, 2003. In the Office Action, the Examiner rejected claims 62-70 under 35 U.S.C. § 102. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

1. Applicant has cancelled claims 1-61 and 71-83, and added new claims 84-97. Claims 62-70 and 84-97 remain pending in this application.

Election/Restrictions

3. Claims 1-61 and 71-83 have been canceled in view of the Examiner's restriction and applicant's subsequent election. Applicant retains the right to present these claims in divisional applications.

Applicant respectfully submits that newly added claims 84-97 are drawn to elected invention III.

Rejections Under 35 U.S.C. § 102

5. The Examiner rejects claims 62-70 under 35 U.S.C. § 102(e) as being anticipated by Levy et al. (US 2001/0004755).

Regarding claim 62, the Examiner asserts that Levy discloses:

an instruction delivery engine to store and fetch instructions either from one or more threads based upon a current processing mode (page 4, paragraph 0059 -- page 5, paragraph 0060); and

an allocator to receive instructions from the instruction delivery engine and to perform allocation in a resource based upon the current processing mode (page 4, paragraph 0059 – page 5, paragraph 0060).

The Examiner provides no specific statement of how the specific claims language reads on the cited portions of Levy. Applicant has carefully reviewed the cited disclosure of Levy and is unable to identify anything that even remotely appears to disclose the use of a current processing mode or performing allocation in a resource based upon the current processing mode. Applicant respectfully requests that the Examiner explain with more specificity how Levy discloses these elements of the claimed invention if the Examiner intends to maintain this rejection.

Regarding claim 63, the Examiner asserts that Levy discloses the processor of claim 62 wherein the allocator assigns the entire resource to the thread that is active if the current processing mode is single threading (page 8, paragraph 0089, 0091 -- 0092, and page 14, paragraph 0141).

Regarding claim 64, the Examiner asserts that Levy discloses the processor of claim 62 wherein the allocator assigns a portion of the resource to each of the threads running

concurrently if the current processing mode is multithreading (page 6, paragraph 0077, page 8, paragraph 0091 -- 0092, and page 14, paragraph 0141).

Applicant has amended claim 63 to include claim 64 and cancelled claim 64. Applicant understands the portions of Levy cited by the Examiner as disclosing claim 63 to disclose the Fully Shared Register (FSR) scheme for allocating registers wherein all registers are managed as a single pool. Page 6, paragraph 0074. Applicant respectfully submits that the allocation disclosed by Levy is distinctly different than the assignment of the claimed invention. As disclosed by the specification at least on page 18, line 25, through page 21, line 2, assignment of resources by the allocator makes those resources available exclusively to the thread to which they are assigned. What Levy discloses is a flexible scheme that can use all of the pooled resources for a single thread if that is the only thread that is running. Page 8, paragraph 0089. Levy does not disclose a processor having a single threading and a multithreading mode nor assigning resources based on such a mode.

Regarding claim 65, the Examiner asserts that Levy discloses the processor of claim 63 wherein the allocator allocates an amount of entries for the instructions from the active thread in the resource if the resource has sufficient available entries and wherein the allocator activates at least one stall signal if the resource does not have sufficient available entries (page 7, paragraph 0084, page 11, paragraph 0120, and page 8, table 3).

Regarding claim 66, the Examiner asserts that Levy discloses the processor of claim 64 wherein the allocator allocates an amount of entries for the instructions from each respective thread in the respective portion if the respective portion has sufficient available entries and wherein the allocator activates at least one stall signal if the respective portion does not have sufficient available entries (page 7, paragraph 0084, page 11, paragraph 0120, and page 8, table 3).

Applicant has amended claim 65 to include claim 66 and cancelled claim 66. Applicant respectfully submits that Levy does not disclose a processor having a single threading and a multithreading mode nor allocating resources based on such a mode.

Regarding claim 67, the Examiner asserts that Levy discloses the processor of claim 66 wherein the instruction delivery engine uses the at least one stall signal to perform its corresponding function (page 7, paragraph 0084, page 11, paragraph 0120, and page 8, table 3). Applicant respectfully disagrees. Applicant understands the cited portions of Levy to disclose instruction fetch stalling generally as a condition that can occur in a processor. However, nothing in Levy discloses an instruction delivery engine using a stall signal activated by an allocator to perform the instruction delivery engine's corresponding function. Applicant has amended claim 67 to depend from claim 65.

Regarding claim 68, the Examiner asserts that Levy discloses the processor of claim 67 wherein the instruction delivery engine re-fetches the stalled instructions in the respective thread to the allocator if the at least one stall signal is activated (page 5-6, paragraph 0068, and page 7, paragraph 0084). Applicant respectfully disagrees. Applicant understands the cited portions of Levy to disclose replaying instructions on an exception in speculative execution of branches and

to separately disclose instruction fetch stalling generally as a condition that can occur in a processor. However, nothing in Levy discloses refetching stalled instructions.

Regarding claim 69, the Examiner asserts that Levy discloses the processor of claim 67 wherein the instruction delivery engine fetches a subsequent instruction from another thread to the allocator if the at least one stall signal for the respective thread is activated and said another thread is not stalled (page 4, paragraph 0053, page 7, paragraph 0084, page 11, paragraph 0120, and page 8, table 3). Applicant respectfully disagrees. Applicant finds nothing in the cited portions of Levy that discloses fetching an instruction from another thread if there is a stall.

Regarding claim 70, the Examiner asserts that Levy discloses the processor of claim 67 wherein the instruction delivery engine fetches an invalid instruction to the allocator if the stall signal for the respective thread is activated (page 10, paragraph 0115). Applicant respectfully disagrees. Applicant finds nothing in the cited portions of Levy that discloses fetching an invalid instruction if there is a stall.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 62-70 under 35 U.S.C. § 102(e) as being anticipated by Levy.

6. The Examiner rejects claims 62-70 under 35 U.S.C. § 102(e) as being anticipated by Rodgers et al. (US 6,496,925).

Applicant has amended the specification to claim the benefit of the earlier filing date of Application No. 09/458,544, filed December 9, 1999, now U.S. Patent No. 6,496,925 to Rodgers et al., under 37 CFR § 1.78. The present application is a continuation-in-part of the earlier filed, co-pending '544 application.

Since the Examiner asserts that Rodgers anticipates the claims of the present application, the Examiner implies that Rodgers provides support for the claims of the present application. Therefore the pending claims of the present application are entitled to the filing date of Rodgers and Rodgers is no longer prior art as to the claims of the present application.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 62-70 under 35 U.S.C. § 102(e) as being anticipated by Rodgers.

Information Disclosure Statement

Applicant respectfully brings to the Examiner's attention an unconsidered Information Disclosure Statement filed on January 2, 2002. A duplicate copy of this filing will be furnished shortly for the Examiner's convenience in the event that the original filing has been misplaced.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: November 20, 2003 By_____

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